

Application No.: 09/752,243

Amendment dated: March 1, 2006

Reply to Office Action dated: December 1, 2005

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A zero generating apparatus comprising An apparatus comprising:
a physical zero register which reads is to read as a zero value and is to be used with an instruction set architecture without a dedicated zero register;
a Register Alias Table (RAT) for storing to store an instruction register map; and
a Zeroing Instruction Logic (ZIL) unit for detecting to detect a zeroing instruction and modifying modify said RAT with a pointer to said physical zero register.
2. (Original) An apparatus in accordance with claim 1, wherein:
said physical zero register is a read only memory (ROM).
3. (Currently Amended) An apparatus in accordance with claim 1, wherein:
said ZIL unit detects is to detect said zeroing instruction in a trace cache line.
4. (Currently Amended) An apparatus in accordance with claim 3, wherein:
an r0 register field logically coupled to said trace cache line for mapping to map to said physical zero register.
5. (Currently Amended) An apparatus in accordance with claim 3, wherein:
said RAT and said trace cache line are logically coupled to a renaming unit for maintaining to maintain said pointer to said physical zero register.

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6. (Currently Amended) An apparatus in accordance with claim 3, wherein:
said ZIL unit deletes is to delete said zeroing instruction from said trace cache line.
7. (Currently Amended) An apparatus in accordance with claim 6, wherein:
said ZIL unit modifies is to modify a subsequent instruction, where said subsequent instruction is logically coupled to said zeroing instruction within said trace cache line.
8. (Currently Amended) An apparatus in accordance with claim 7, wherein:
said ZIL unit modifies is to modify said subsequent instruction with an immediate source of zero.
9. (Original) An apparatus in accordance with claim 1, wherein:
said zeroing instruction is an exclusive or (XOR).
10. (Original) An apparatus in accordance with claim 1, wherein:
said zeroing instruction is a subtraction (SUB).
11. (Original) An apparatus in accordance with claim 1, wherein:
said zeroing instruction is a multiply (MUL).
12. (Original) An apparatus in accordance with claim 1, wherein:
said zeroing instruction is a move (MOV).

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13. (Currently Amended) An apparatus in accordance with claim 7, wherein:

said ZIL unit transforms is to transform said subsequent instruction to a MOV instruction.

14. (Currently Amended) A zero-generating apparatus for use with a microprocessor, comprising An apparatus comprising:

a physical zero register which is to read as a zero value to be used with an instruction set architecture without a dedicated zero register;

a Zeroing Instruction Logic (ZIL) unit to read a plurality of instructions and to detect and modify a zeroing instruction within said plurality of instructions;

where said ZIL unit is to delete said zeroing instruction and set a pointer to said physical zero register in place of said deleted zeroing instruction; and

where said ZIL unit is to modify instructions dependent on said deleted zeroing instruction.

15. (Previously Presented) An apparatus in accordance with claim 14, wherein:

said ZIL unit is to modify instructions dependent on said deleted zeroing instructions with an immediate source of a value when both occur with a single trace cache line.

16. (Previously Presented) An apparatus in accordance with claim 14, wherein:

said ZIL unit is to modify instructions dependent on said deleted zeroing instructions with a renameable pointer.

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17. (Currently Amended) A method of zero-generating comprising A method comprising:
detecting a zeroing instruction in an instruction set architecture ~~without~~ not including a
dedicated zero register;
deleting said zeroing instruction;
identifying a subsequent instruction using said zeroing instruction; and
modifying said subsequent instruction with a pointer to a physical zero register which
reads as a zero value.

18. (Original) A method in accordance with claim 17, further comprising:
pointing to a physical zero register where said subsequent instruction is not within a
common trace cache line.

19. (Currently Amended) A method in accordance with claim 17, further comprising:
wherein:
modifying said subsequent instruction ~~involves~~ includes replacing instruction sources.

20. (Currently Amended) A method in accordance with claim 17, further comprising:
wherein:
modifying said subsequent instruction ~~involves~~ includes using a move (MOV)
instruction.

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21. (Original) A method in accordance with claim 17, further comprising:
said subsequent instruction is modified in response to its location in a trace cache relative
to said zeroing instruction.